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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,289	01/04/2002	Gilbert Wolrich	10559-612001/P12851	8345

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EXAMINER	
CHANNAVAJJALA, SRIRAMA T	
ART UNIT	**PAPER NUMBER**
2164	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,289	WOLRICH ET AL.	
	Examiner	Art Unit	
	Srirama Channavajjala	2164	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1-30 are pending in this application.

2. Examiner acknowledges applicant's amendment filed on 8/12/2004.

3. In view of applicant's amendment to claim 20, the objection to the claim 20 as set forth in the previous office action is hereby withdrawn.

4. In view of applicant's submitted arguments [see page 10-11], the rejection of claims 1-25 under 35 USC 101 set forth in the previous office action is hereby withdrawn

5. In view of applicant's filed "Terminal Disclaimer under 37 CFR 3.73(b) and 1.32(b), the non statutory double patenting rejection set forth in the previous office action is hereby withdrawn.

Drawings

6. Examiner acknowledges applicant filed drawings are acceptable for examination, and in view of applicant's amendment to the figs 2-4, the objection to the drawings set forth in the previous office action is hereby withdrawn.

Information Disclosure Statement

7. The electronic information disclosure statement (eIDS) submitted on 28 June 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner, a copy of electronic information disclosure statement [1-7 pages] enclosed with this office action.

Specification

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) ***BRIEF SUMMARY OF THE INVENTION.***
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

8. In the specification, "BRIEF SUMMARY OF THE INVENTION" is missing. Applicant is hereby required to provide *"BRIEF SUMMARY OF THE INVENTION"* in response to this office action. See 37 CFR 1.77(b),

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Slane, US Patent No. 6438651.

10. As to Claim 1, 26, Slane teaches a system which including 'storing in memory a queue descriptor including a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue' [col 3, line 40-42]; 'in response to a command to perform an enqueue or dequeue operation with respect to the queue, fetching from the memory to a cache one of either the head pointer or tail pointer' [col 2, line 23-26, col 3, line 52-61, fig 2], Slane teaches queue operations, more specifically enqueue, dequeue operations to the queue as detailed in fig 2, further Slane also teaches memory element 60 having a data structure that contains head and tail pointers elements 64 and 66 as detailed in fig 2; 'returning to the memory from the cache portions of the queue descriptor modified by the operation' [col 4, line 4-8].

11. As to Claim 2, 15, Slane disclosed 'fetching the head pointer and not the tail pointer in response to a command to perform a dequeue operation' [col 3, line 52-55, col 4, line 47-49, col 5, line 61-63, fig 3].

12. As to Claim 3, 16, Slane disclosed 'fetching the tail pointer and not the head pointer in response to a command to perform an enqueue operation' [col 4, line 47-51, fig 3].

13. As to Claim 4, 17, Slane disclosed 'returning to memory the head pointer and not the tail pointer if only dequeue operations were performed on the queue'[col 4, line 51-52, line 56-60, fig 4-6].

14. As to Claim 5, 18, Slane disclosed 'returning to memory the tail pointer and not the head pointer if only enqueue operations were performed on the queue while the queue was unempty' [col 5, line 64-67, col 6, line 1-8].

15. As to Claim 6, 19, Slane disclosed 'returning to memory the head pointer and tail pointer if an enqueue and a dequeue operation were performed on the queue, or an enqueue operation was performed on the queue while the queue was empty' [col 7, line 3-8].

16. As to Claim 7, Slane teaches a system which including 'determining whether a head pointer or a tail pointer of a queue descriptor that was fetched from memory to a cache had been modified by an enqueue or a dequeue operation' [fig 2, col 3, line 52-66, col 4, line 37-47], Slane is directed to managing requests to a cache using flags to queue and dequeue data, more specifically optimizing read and write events for queues [see Abstract], further it is noted that Slane also specifically directed to queue operations that including enqueue, dequeue operations with respect to main memory using tail and head pointers [see fig 2]; 'returning a particular pointer to the memory from the cache only if that pointer had been modified' [col 4, line 56-62].

17. As to Claim 8, 20, Slane disclosed 'using valid bits in the cache to track modifications to the pointers' [col 6, line 19-25].

18. As to Claim 9, 21, Slane disclosed 'using a first valid bit to track modifications to the head pointer and second valid bit to track modifications to the tail pointer' [col 6, line 26-37].

19. As to Claim 10, 22, 29, Slane disclosed 'setting the first valid bit if a dequeue operation is performed with respect to the queue descriptor' [col 6, line 57-64], 'an enqueue operations performed with respect to the queue descriptor while the queue is empty' [col 7, line 3-12].

20. As to Claim 11, 23, Slane disclosed 'setting the second valid bit if an enqueue operation is performed with respect to the queue descriptor' [col 4, line 65-67, col 5, line 1-8].

21. As to Claim 12, 24, Slane disclosed 'setting a pointer's valid bit when the pointer is fetched from the memory to the cache' [col 5, line 55-63].

22. As to Claim 13, 25, 30, Slane disclosed 'returning to the memory pointers whose valid bits have been set' [col 5, line 59-63].

23. As to Claim 14, Slane teaches a system which including 'memory for storing queue descriptors which include a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue' [fig 2, col 3, line 40-42, line 52-57]; 'a cache for storing queue descriptors corresponding to up to a number of the memory's queue descriptors' [col 3, line 40-42 line, 58-61], 'a processor configured to: fetch from the memory to the cache one of either the head pointer or the tail pointer of a particular queue descriptor in response to a command to perform an enqueue or a dequeue operation with respect to the particular queue descriptor' [col 2, line 23-26, col 3, line 52-61, fig 2], Slane teaches queue operations, more specifically enqueue, dequeue operations to the queue as detailed in fig 2, further Slane also teaches memory element 60 having a data structure that contains head and tail pointers

elements 64 and 66 as detailed in fig 2; 'return to the memory from the cache portions of the queue descriptor modified by the operation' [col 4, line 4-8].

24. As to Claim 27, Slane disclosed 'fetch the head pointer and not the tail pointer in response to a command to perform a dequeued operation' [col 3, line 52-55, col 4, line 47-49, col 5, line 61-63, fig 3], 'fetching the tail pointer and not the head pointer in response to a command to perform an enqueue operation' [col 4, line 47-51, fig 3].

25. Slane disclosed 'returning to memory the head pointer and not the tail pointer if only dequeue operations were performed on the queue'[col 4, line 51-52, line 56-60, fig 4-6].

26. As to Claim 28, Slane disclosed 'the head pointer and not the tail pointer if only dequeue operations are performed on the queue'[col 4, line 51-52, line 56-60, fig 4-6], 'the tail pointer and not the head pointer if only enqueue operations are performed on the queue while the queue was unempty' [col 5, line 64-67, col 6, line 1-8], 'the head pointer and tail pointer if both an enqueue and a dequeue are performed on the queue, or an enqueue operation was performed on the queue while the queue was empty' [col 7, line 3-8].

Response to Arguments

27. Applicant's arguments filed 8/12/2004 with respect to claims 1-30 have been fully considered but they are not persuasive, for examiner's response, see discussion below:

a) At page 11, claims 1-6 applicant argues that Slane neither describes nor suggests at least "fetching from the memory to a cache one of either the head pointer or tail pointer"

As to the argument [a], Slane is directed to managing requests to a cache using flags to queue and dequeue data in a buffer, more specifically managing read and write requests to cache to process enqueue and dequeue operations [se Abstract], Slane also discussed circular buffer operates based on first in first out or FIFO arrangement especially utilizing tail and head pointers to manage data entry [see col 1, line 38-58], further it is noted that Slane specifically teaches data blocks are fetched from the memory that including the specific request data block to access.
Slane also teaches main memory including circular buffer data structure having head and tail pointers as detailed in fig 2, examiner interpreting head and tail pointers corresponds to fig 2, element 64, and 66 respectively. Therefore, Slane teaches fetching data from the memory to the cache one of either the head pointer or tail pointer because the main memory data structure including circular buffer data structure having head and tail pointers [see col 3, line 40-44, line 52-61, fig 2].

Examiner applies above arguments to claim 26.

b) At page 11, claims 7-13, applicant argues that since Slane neither discloses nor suggests at least "determining whether a head pointer or a tail pointer of a queue descriptor that was fetched from memory to a cache had been modified"

As to the above argument [b], Slane is directed to managing requests to a cache using flags to queue and dequeue data, more specifically optimizing read and write events for queues [see Abstract], further it is noted that Slane also specifically directed to queue operations that including enqueue, dequeue operations with respect to main memory using tail and head pointers [see fig 2]. As best understood by the examiner, Slane specifically suggests head and tail pointers are provided with specific addresses for determine data entry in the data blocks, and when entries are in the enqueued or added to the circular buffer, the data is then written to cache as detailed in col 4, line 41-47, Slane also further suggests that because the data structure is a circular buffer, dequeue requests will be for data at the head and enqueue requests will be for a data block following the most recently added data block to the circular buffer that corresponds to circular buffer is modified as detailed in col 4, line 47-51.

c) At page 11, claims 14-25, applicant argues that since Slane neither discloses nor suggests at least "an article comprising a computer –readable medium that stores computer.....fetch from memory to a cache one of either a head pointer.....

As to the above argument, examiner applies above discussed arguments, further it is noted that Slane specifically disclosed computing environment that includes a queue which may comprise a processor unit, CPU, hardware etc., as detailed in col 3, line 29-36, fig 2].

d) At page 11, line 22-24, applicant argues that nowhere in the cited portions of Slane, or anywhere in Slane, are either elements 64 or 66 fetched from a memory to a cache.

As to the above argument [d], Slane teaches data structure, more specifically main memory includes circular buffer data structure having head and tail pointers as detailed in fig 2, col 3, line 40-42.

Conclusion

The prior art made of record

a. US Patent No. 6438651

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

b. US Patent No. 5268900

c. US Patent No. 5684962

d. US Patent No. 6351474

e. US Patent No. 6684303

f. US Patent No. 2002/0144006

g. US Patent No. 2002/0131443

h. EP0418447

i. Eric A Brewer et al., "Remote queue: exposing message queues for optimization and atomicity, appears in SPAA '95 Santa Barbara, CA pp 1-13

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srirama Channavajjala whose telephone number is 571-272-4108. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popvici, can be reached on 571-272-.4083. The fax phone numbers for the organization where the application or proceeding is assigned is 703/872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)

sc
Patent Examiner.
November 12, 2004.

SRIRAMA CHANNAVAJJALA
PRIMARY EXAMINER